Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte FUKASHI MORISHITA

Appeal No. 2004-2120
Application No. 09/987,566

HEARD: March 8, 2005

Before HAIRSTON, BARRETT, and LEVY, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 19 and 20.

The disclosed invention relates to a level detecting circuit for detecting a difference between a first voltage and second voltage.

Claim 19 is the only independent claim on appeal, and it reads as follows:

19. Level detection circuitry for detecting a difference between a first voltage and a second voltage, comprising:

said first insulated gate transistor receiving a power supply voltage as the first voltage at a gate thereof and having a first conduction node, and a second conduction node for outputting a difference signal, and

said second insulated gate transistor receiving a reference voltage as the second voltage at a gate thereof and having a first conduction node connected to said first conduction node of said first insulated gate transistor, said second insulated gate transistor having a current supply ability different from a current supply ability of said first insulated gate transistor under a condition of the same gate voltage, and said difference signal corresponding to a difference between the first and second voltages, said reference voltage determining a voltage level of an internal voltage generated from said power supply voltage;

operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, said operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

a buffer circuit for buffering said difference signal for generating a binary level detection signal indicating whether said first voltage is higher than said second voltage.

The reference relied on by the examiner is:

Bion et al. (Bion)	5,862,091	Jan. 19, 1999 (filed July 22, 1997)

Claims 19 and 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Bion.

Reference is made to the briefs (paper numbers 14 and 17) and the answer (paper number 15) for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the anticipation rejection of claims 19 and 20.

Anticipation is established when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of the claimed invention. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

The examiner is of the opinion (final rejection, 2 and 3) that the comparator circuit 37 in Bion (Figures 11 and 12; column 8, lines 45 through 56) discloses all of the circuit elements set forth in claims 19 and 20. Appellant argues throughout the briefs that Bion fails to disclose the limitations of "said reference voltage determining a voltage level of an internal voltage generated from said power supply voltage," and "a buffer circuit for buffering said difference signal for generating a binary level detection signal indicating whether said first voltage is higher than said second voltage." In response, the examiner contends that the voltage input on one of the inputs to the comparator 37 functions as a reference voltage to the power supply voltage input (Vcc) on the other input to the comparator (answer, page 6), and that the buffer 44 will provide a binary indication (answer, pages 6 and 7).

We agree with the examiner that the broadly recited function of the reference voltage determining a voltage level of an internal voltage generated from the power supply voltage is met by the comparison of the two voltage inputs to the comparator 37. The result of the comparison is "internal" to the comparator, and it is a voltage value dependent upon one of the input voltage values being treated as a "reference voltage" value in the comparison to the power supply voltage Vcc. On the other hand, we agree with the appellant that Bion is completely silent as to the high-gain amplifier 44 functioning to generate a "binary" level detection signal. Bion merely teaches that the amplifier operates as a buffer-type shaping circuit that amplifies "the current difference present in the two arms of the differential stage [37]" (column 8, lines 41 through 44).

Thus, the anticipation rejection of claims 19 and 20 is reversed for lack of a teaching in Bion of a "binary" signal output from the amplifier 44.

DECISION

The decision of the examiner rejecting claims 19 and 20 under 35 U.S.C. § 102(e) is reversed.

REVERSED

KENNETH W. HAIRSTON
Administrative Patent Judge

LEE E. BARRETT
Administrative Patent Judge

STUART S. LEVY
Administrative Patent Judge

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KWH/lp

McDERMOTT, WILL & EMERY
600 13th STREET, N.W.
WASHINGTON, DC 20005-3096